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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/898,583	HENRY ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-52 have been examined.

Papers Received

2. Receipt is acknowledged of the amendment papers submitted, where the papers have been placed of record in the file.

3. The amendment has successfully overcome the objections to the specification and drawings as well as the 35 USC 112 rejections, all of which are withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6, 10, 12-15, 18-24, 26-32, 38-43, and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Isaman (6,035,391).

6. In regard to claim 1, Isaman discloses a branch control apparatus in a microprocessor, comprising:

a. an instruction cache, for outputting a line of instruction bytes selected by a fetch address (figure 1, element 16 and figure 3, element 104);

b. an instruction buffer, coupled to said instruction cache, for buffering said line of instruction bytes; [Figure 3 shows multiple parcel registers 108A-108C, which buffer parsed instructions, that is separate bytes of the instruction line.

Thus parcel register 108A, for example, is an instruction buffer that buffers instruction bytes of a line of instructions from the cache.]

c. a branch target address cache, coupled to said fetch address, for providing offset information relating to a location of a branch instruction within said line of instruction bytes; [Figure 1, element 18, column 4, lines 65-66, and column 9, lines 6-15 show a branch target buffer or BTB. The included dictionary definition shows that in a processor using branch prediction a BTB stores the predicted destination (or target address). Thus functionality is used as given in the sections and figure above along with the fetch address to provide target addresses or offsets to the instruction cache to fetch from. When the target line pointed to by the target address contains a branch instruction, the offset or target address relates to a location of the branch instruction within that cache line of instruction bytes.]

d. and selection logic, coupled to said BTAC, for causing a portion of said instruction bytes not to be provided to said instruction buffer, based on said offset information. [As shown in figure 3 and column 8, lines 1-13, the instruction parser separates the instruction line into separate instruction buffers or parcel registers. Thus certain instruction bytes are not provided to instruction buffer 108A, for example. This parsing is based on the BTAC or BTB offset information when the BTAC or BTB unit provided the offset or target address for which to fetch the current line of instructions.]

7. In regard to claim 2, Isaman discloses the apparatus of claim 1, wherein said offset information specifies a location of an instruction immediately following said branch instruction within said line of instruction bytes. [As given above, the offset or target address gives the entire line of instructions (or RISC OP parcels as given in column 8, lines 13) and thus specifies both the branch instruction and the instruction after it when the branch is not the last instruction in the line.]

8. In regard to claim 3, Isaman discloses the apparatus of claim 2, wherein said portion of said instruction bytes not provided to said instruction buffer comprises instruction bytes immediately following said branch instruction within said line of instruction bytes as specified by said offset. [Since the parcels are separate instructions (RISC operations) each instruction after the branch instruction will be provided to a different instruction buffer or parcel register and thus not provided to say the first instruction buffer.]

9. In regard to claim 4, Isaman discloses the apparatus of claim 1, wherein said selection logic comprises: a register coupled between said instruction cache and said instruction buffer, for storing said line of instruction bytes. [The instruction parser 22 of figure 3 inherently contains a register to hold the incoming instruction line to be parsed since the parsing function is a pipeline stage as given in figure 2.]

10. In regard to claim 5, Isaman discloses the apparatus of claim 4, wherein said selection logic further comprises: a plurality of valid bits coupled to said register, wherein each of said plurality of valid bits is associated with of said instruction bytes in said register. [The register inherently receives and sends bits that are valid (at some

point in time or the processor would have no use) and are thus are coupled to the register. The claim states "valid bits", which simply requires that the bits are somehow associated with valid information whether the bits be valid themselves or indicate validity of other bits.]

11. In regard to claim 6, Isaman discloses the apparatus of claim 5, wherein said selection logic populates said plurality of valid bits based on said offset information received from said BTAC. [As given above, the instruction line is based on the offset information and thus these instruction bytes, when valid and transferred to the register, are the valid bytes based on the offset.]

12. In regard to claim 10, Isaman discloses the apparatus of claim 5, wherein said selection logic further comprises: muxing logic, coupled between said instruction cache and said instruction buffer, for causing ones of said instruction bytes indicated as valid by said associated valid bit to be provided to said instruction buffer. [Since muxing logic is known in the art to be simply selection logic, the selection logic is the muxing logic for sending instruction bytes to the instruction buffer from a cache holding instruction bytes. Since the bytes may be viewed as the valid bits, which are each associated with each other, a valid instruction byte or parcel is provided to the first buffer.]

13. In regard to claim 12, Isaman discloses the apparatus of claim 10, wherein said muxing logic comprises a set of muxes for aligning ones of said instruction bytes indicated as valid by said associated valid bit with a first empty location in said instruction buffer. [As given above, the selection logic or muxes select or align the valid

instruction bytes to various instruction buffers. AN empty location inherently receives the bytes.]

14. In regard to claim 13, Isaman discloses the apparatus of claim 10, wherein said muxing logic comprises a set of muxes for shifting ones of said instruction bytes indicated as valid by said associated valid bit by a number of bytes shifted out of said instruction buffer. [It is inherent that if a byte of the instruction buffer is shifted out and a new instruction byte is ready that the muxes will shift that new instruction byte into the buffer.]

15. In regard to claim 14, Isaman discloses the apparatus of claim 13, wherein said selection logic is configured to receive a shift count from instruction format logic for indicating a number of instruction bytes to be shifted out of said instruction buffer. [As given in the sections cited above, the instruction line is broken up into a varying number of parcels or RISC instructions. The bytes of the line serve as a count of the number of parcels that need to be executed and thus shifted out of the instruction buffers or parcel registers. The selection logic itself serves as the instruction format logic since parses and decided how many instructions are shifted to (and thus out of) the instruction buffers.]

16. In regard to claim 15, Isaman discloses the apparatus of claim 14, wherein said muxing logic shifts said ones of said instruction bytes indicated as valid by said associated valid bit by said shift count. [Since the muxing logic receives indication of free instruction bytes, the muxing logic selects appropriate instruction byte for shifting into the buffer (which only holds valid bytes).]

17. In regard to claim 18, Isaman discloses the apparatus of claim 1, wherein said instruction buffer is directly coupled to instruction format logic that formats said instruction bytes. [The decoder, which is format logic since it interprets the instruction bytes into a more readable format, is directy coupled to the instruction buffer or parcel register as shown in figure 3.]

18. In regard to claim 19, Isaman discloses the apparatus of claim 18, wherein a bottom byte of said instruction buffer is provided directly to a portion of said instruction format logic configured to a first byte of an instruction for formatting. [See figure 3.]

19. In regard to claim 20, Isaman discloses the apparatus of claim 1, wherein said branch instruction comprises an x86 branch instruction. [Column 5, lines 34 – 54 show that the instruction cache holds x86 instructions and thus the branches must be x86 branches.]

20. In regard to claim 21, Isaman discloses the apparatus of claim 1, wherein said BTAC is configured to provide a target address of said branch instruction in response to said fetch address. [As previously described.]

21. In regard to claim 22, Isaman discloses the apparatus of claim 21, wherein said target address is selectively provided to said instruction cache as a subsequent fetch address for selecting a second line of instruction bytes containing a target instruction of said branch instruction in said instruction cache. [As given previously.]

22. In regard to claim 23, Isaman discloses the apparatus of claim 22, wherein said selection logic cause said target instruction to be provided to said instruction buffer adjacent to said branch instruction within said instruction buffer. [As given above, each

parcel register or instruction buffer receives a separate RISC instruction and thus the target instruction if speculatively fetched with the branch instruction will be in the buffer adjacent the branch instruction's buffer.]

23. In regard to claim 24, Isaman discloses the apparatus of claim 23, wherein said selection logic causes instruction bytes preceding said target instruction in said second line to be discarded and not provided to said instruction buffer. [As given above, each instruction goes to a different buffer and thus the preceding instructions will not be provided to the same buffer as the branch instruction.]

24. Claims 26-32, 38-43, and 45 are substantially similar to the limitations given in claims 1-26 and thus the same arguments given for those claims apply here as well.

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 7-9, 11, 44, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaman.

27. In regard to claim 7,

a. Isaman discloses the apparatus of claim 6.

b. Isaman does not explicitly disclose wherein said selection logic causes each of said instruction bytes in said register having a corresponding valid bit that

indicates said corresponding instruction byte is invalid to not be provided to said instruction buffer.

c. The examiner is taking Official Notice that it is well known in the art to have a corresponding valid bit to an instruction byte to indicate whether it is valid or not and if not valid to refrain the instruction from being provided to the instruction buffer for issuance and execution.

d. One of ordinary skill in the art would have recognized that checking instructions for validity and not allowing invalid instructions to execute would allow for data integrity to be maintained.

It would have been obvious to one of ordinary skill in the art to modify the design of Isaman to check instructions for validity and not allowing invalid instructions to execute so that data integrity would have been maintained.

28. In regard to claim 8, Isaman discloses the apparatus of claim 7, wherein said BTAC provides a hit signal to said selection logic for indicating whether or not said fetch address hit in said BTAC. [As shown in the sections cited above, the BTB or BTAC indicates a fetch address based on a prediction (hit or miss signal) so that the fetch and select logic fetches the right instructions.]

29. In regard to claim 9, Isaman discloses the apparatus of claim 8, wherein said selection logic populates said plurality of valid bits based on said offset information received from said BTAC if said hit signal indicates said fetch address hit in said BTAC. [As shown above, the instruction bytes can be viewed as the valid bits, which are

populated based on the BTAC and the instructions indicated to fetch based on a hit signal.]

30. In regard to claim 11,

a. Isaman discloses the apparatus of claim 10, wherein said muxing logic comprises a set of muxes. Again, since muxes and selection logic are synonymous, the logic is made up of muxes.

b. Isaman does not explicitly disclose wherein said set of muxes is for discarding ones of said instruction bytes indicated as invalid by said associated valid bit

c. The examiner is taking Official Notice that it is well known in the art to have a corresponding valid bit to an instruction byte to indicate whether it is valid or not and if not valid to refrain the instruction from being provided to the instruction buffer for issuance and execution.

d. One of ordinary skill in the art would have recognized that checking instructions for validity and not allowing invalid instructions to execute would allow for data integrity to be maintained.

It would have been obvious to one of ordinary skill in the art to modify the design of Isaman to check instructions for validity and not allowing invalid instructions to execute so that data integrity would have been maintained.

31. Claims 44 and 46 are substantially similar to the claimed subject matter given above and thus the same arguments apply here.

32. Claims 16-17 and 33-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaman in view of Schwendiger (6,250,821).

33. In regard to claim 16,

a. Isaman discloses the apparatus of claim 1,

b. Isaman does not disclose wherein said instruction buffer comprises a shift register.

c. Schwendiger discloses an apparatus for processing branch instructions that includes an instruction buffer that comprises a shift register to store instructions before sent to a decoder as shown in the abstract.

d. Column 1, line 66 – column 2, line 14 show that the invention of Schwendiger allows for more versatility and is able to accept more instructions from memory at a time resulting in speedup compared to the prior art. This versatility and speedup would have motivated one of ordinary skill in the art to modify the design of Isaman to include the instruction buffer of Schwendiger that uses a shift register.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Isaman to use the instruction buffer disclosed by Schwendiger that embodies a shift register so that greater versatility and system speed is realized.

34. In regard to claim 17, Isaman in view of Schwendiger discloses the apparatus of claim 16, wherein said shift register is one byte-wide. Column 4, lines 61-63 show that four 32-bit (4-byte) instructions are sent to lines of the shift register instruction buffer

and thus the shift register is at least one byte wide (that is, one byte plus three others as is allowed by the open ended transition phrase of "wherein").

35. In regard to claim 33,

a. Isaman discloses the pre-decode stage of claim 26,

b. Isaman does not disclose wherein said instruction buffer comprises a shift register.

c. Schwendiger discloses an apparatus for processing branch instructions that includes an instruction buffer that comprises a shift register to store instructions before sent to a decoder as shown in the abstract.

d. Column 1, line 66 – column 2, line 14 show that the invention of Schwendiger allows for more versatility and is able to accept more instructions from memory at a time resulting in speedup compared to the prior art. This versatility and speedup would have motivated one of ordinary skill in the art to modify the design of Isaman to include the instruction buffer of Schwendiger that uses a shift register.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Isaman to use the instruction buffer disclosed by Schwendiger that embodies a shift register so that greater versatility and system speed is realized.

36. In regard to claim 34, Isaman in view of Schwendiger discloses the apparatus of claim 33, wherein said shift register is one byte-wide. Column 4, lines 61-63 show that four 32-bit (4-byte) instructions are sent to lines of the shift register instruction buffer

and thus the shift register is at least one byte wide (that is, one byte plus three others as is allowed by the open ended transition phrase of "wherein").

37. In regard to claim 35,

a. Isaman in view of Schwendiger discloses the pre-decode stage of claim 33,

b. Isaman in view of Schwendiger does not explicitly disclose wherein said selection logic writes said branch instruction and said target instruction immediately adjacent to a last valid data byte in said instruction buffer.

c. The examiner is taking official notice that a first-in first-out (FIFO) buffer is well and known in the art and it would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Isaman to use a FIFO buffer as the instruction buffer disclosed therein so that a simple buffer model is utilized. With this FIFO buffer in place it would be inherent that the branch and target instruction are adjacent to the last valid byte in the buffer since that is where the next open space would be.

38. In regard to claim 36, Isaman in view of Schwendiger discloses the pre-decode stage of claim 33, wherein said selection logic writes said branch instruction and said target instruction to a next empty location in said instruction buffer. It is inherent that the instructions are written to an empty location in the buffer and the term "next" is simply a name since no relative position of what the instructions are next to is given.

39. In regard to claim 37, Isaman in view of Schwendiger discloses the pre-decode stage of claim 33, wherein said instruction buffer is directly coupled to said instruction

format logic. Figure 10 shows that the instruction buffer (element 11) is in fact directly coupled to the instruction format logic (elements 16 and 17).

40. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isaman in view of Miller (6,081,884).

41. In regard to claim 25,

a. Isaman discloses the apparatus of claim 1,

b. Isaman does not disclose wherein said instruction cache stores variable length instructions for execution by the microprocessor.

c. Miller had disclosed in the abstract the use of variable length instructions for processing.

d. Miller has shown in column 1, lines 14-16 that variable length instructions allow for efficient utilization of storage space and memory. This efficient utilization of memory would have motivated one of ordinary skill in the art to modify the design of Isaman to use variable length instructions as taught by Miller. Thus the instruction cache (which caches all instructions) now caches variable length instructions.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Isaman to use variable length instructions as taught by Miller so that efficient utilization of memory space is realized.

42. In regard to claim 47,

a. Isaman discloses the apparatus of claim 1,

b. Isaman does not disclose wherein said line of instruction bytes comprises a variable number of instructions.

c. Miller had disclosed in the abstract the use of variable length instructions for processing.

d. Miller has shown in column 1, lines 14-16 that variable length instructions allow for efficient utilization of storage space and memory. This efficient utilization of memory would have motivated one of ordinary skill in the art to modify the design of Isaman to use variable length instructions as taught by Miller. Thus the instruction cache (which caches all instructions) now caches variable length instructions, which yields a variable number of RISC instructions for parsing.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Isaman to use variable length instructions (and thus a variable number of instructions) as taught by Miller so that efficient utilization of memory space is realized.

43. In regard to claim 48,

a. Isaman discloses the apparatus of claim 1,

b. Isaman does not disclose wherein said line of instruction bytes comprises instructions of variable length.

c. Miller had disclosed in the abstract the use of variable length instructions for processing.

d. Miller has shown in column 1, lines 14-16 that variable length instructions allow for efficient utilization of storage space and memory. This efficient utilization of memory would have motivated one of ordinary skill in the art to modify the design of Isaman to use variable length instructions as taught by Miller. Thus the instruction cache (which caches all instructions) now caches variable length instructions.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Isaman to use variable length instructions as taught by Miller so that efficient utilization of memory space is realized.

44. Claims 49 and 51 are basically the same as claim 47 and the same arguments applied to that claim apply here as well.

45. Claims 50 and 52 are basically the same as claim 48 and the same arguments applied to that claim apply here as well.

Response to Arguments

46. Applicant's arguments filed 12/30/04, with respect to the rejections of the claims under 35 USC 102 and 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Isaman.

Conclusion

47. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the

claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:30-4:00 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
April 4, 2005

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